

WHAT IS CLAIMED IS:

- 1 1. A method for testing a radio frequency (RF) circuit comprising:
2 observing a signal from the RF circuit, wherein the signal is a digital signal from within
3 the RF circuit;
4 manipulating the signal; and
5 producing a metric for the test based on results from the manipulating.
- 1 2. The method of claim 1, wherein the testing is performed using built-in self test (BIST)
2 techniques.
- 1 3. The method of claim 1, wherein the signal is a phase error signal.
- 1 4. The method of claim 1, wherein the signal has a high degree of correlation with an RF
2 output of the RF circuit.
- 1 5. The method of claim 4, wherein a transfer function between the signal and the RF output
2 phase is flat within a frequency band of interest.
- 1 6. The method of claim 1, wherein the RF circuit is an all-digital circuit, and wherein the
2 signal is an output of a component in an all-digital phase-locked loop in the RF circuit.
- 1 7. The method of claim 6, wherein the signal is an output of a phase detector.
- 1 8. The method of claim 7, wherein the signal has been filtered.
- 1 9. The method of claim 8, wherein the all-digital phase-lock loop is operating in a type-II
2 mode, and the signal is an output of an integral accumulator of a loop filter.

- 1 10. The method of claim 8, wherein the all-digital phase-lock loop is operating in a type-I
2 mode, and the signal is an output of an infinite impulse response filter coupled to the output of a
3 loop filter.
- 1 11. The method of claim 8, wherein a loop filter coupled to an output of a phase detector
2 performs the filtering, and wherein the signal is an output of the loop filter.
- 1 12. The method of claim 6, wherein the signal is an output of a gain normalization block.
- 1 13. The method of claim 1, wherein the frequency of the signal is several orders of
2 magnitude less than the frequency of the RF output.
- 1 14. The method of claim 1, wherein the test is for phase error trajectory and the signal is the
2 output of a phase detector, and wherein the manipulation comprises measuring a change in the
3 signal.
- 1 15. The method of claim 14, wherein if the change in the signal is less than a specified
2 threshold, then the phase error trajectory is good.
- 1 16. The method of claim 14, wherein the measuring the change in the signal comprises
2 measuring a peak, a variance, or a rate of change in the signal.
- 1 17. The method of claim 1, wherein the test is for frequency lock and the signal is the output
2 of a phase detector, and wherein the manipulation comprises comparing a value of the signal
3 over several samples.
- 1 18. The method of claim 17, wherein if a variance in the magnitude is less than a specified
2 threshold, then the frequency has been locked.

- 1 19. The method of claim 17, wherein the samples are taken at different times.
- 1 20. The method of claim 1, wherein the test is for frequency deviation and the signal is an
2 output of an integral accumulator of a loop filter, and wherein the manipulation comprises
3 comparing the signal with a specified range.
- 1 21. The method of claim 20, wherein if the signal is within the specified range, then the
2 frequency deviation is within acceptable limits.
- 1 22. The method of claim 20, wherein the manipulation further comprises comparing several
2 samples of the signal.
- 1 23. The method of claim 20, wherein the RF circuit contains an all-digital phase-locked loop
2 operating in a type-II mode.
- 1 24. The method of claim 1, wherein the RF circuit contains an all-digital phase-locked loop,
2 and the method further comprises prior to the observing, setting the all-digital phase-locked loop
3 to a certain bandwidth.
- 1 25. The method of claim 24, wherein the test is for estimating phase noise power and the
2 signal is an output of a phase detector, and wherein the manipulating comprises calculating a
3 mean square error of the signal.
- 1 26. The method of claim 25, wherein the setting, observing, and manipulating is repeated for
2 several different all-digital phase-locked loop bandwidths, and wherein the producing comprises
3 subtracting the calculated mean square errors for the several different all-digital phase-lock loop
4 bandwidths.

1 27. The method of claim 1, wherein the RF circuit is an all-digital frequency synthesizer.

1 28. The method of claim 1, wherein the RF circuit is an all-digital transmitter.

1 29. The method of claim 28, wherein the transmitter is used in a wireless communications
2 network.

1 30. The method of claim 29, wherein the wireless communications network is Bluetooth
2 compliant.

1 31. The method of claim 1, wherein the testing comprises a functional test or a compliance
2 test of the RF circuit.

- 1 32. A circuit comprising:
2 a processor coupled to a radio frequency (RF) circuit, the processor containing circuitry
3 to manipulate digital signals from the RF circuit to provide a performance metric for the RF
4 circuit; and
5 a control signal input coupled to the processor, wherein the control signal input can
6 enable an observation and manipulation of the digital signals.
- 1 33. The circuit of claim 32 further comprising a latch coupled to the processor, the latch to
2 store the performance metric provided by the processor.
- 1 34. The circuit of claim 32, wherein the RF circuit is integrated onto a first integrated circuit,
2 wherein the processor is integrated onto a second integrated circuit.
- 1 35. The circuit of claim 34, wherein the first and the second integrated circuits are the same
2 integrated circuit.
- 1 36. The circuit of claim 32, wherein the RF circuit contains an all-digital phase-locked loop,
2 and wherein the processor is coupled to an output of a phase detector.
- 1 37. The circuit of claim 32, wherein the RF circuit contains an all-digital phase-locked loop,
2 and wherein the processor is coupled to a filtered output of a phase detector.
- 1 38. The circuit of claim 32, wherein the RF circuit contains an all-digital phase-locked loop,
2 and wherein the processor is coupled to an output of a phase detector and a filtered output of a
3 phase detector.

1 39. The circuit of claim 32, wherein the circuit permits the testing of the RF circuit in wafer,
2 in packaged integrated circuit, in factory, and in field.

1 40. The circuit of claim 32, wherein the circuit permits the testing of the RF circuit, and
2 wherein the testing is of a type selected from a group consisting of a phase trajectory error, a
3 frequency lock, a frequency deviation, a phase noise power, or combinations thereof.

1 41. A circuit comprising:
2 a reference phase accumulator coupled to a signal input, the reference phase accumulator
3 containing circuitry to compute a reference phase;
4 a phase detector coupled to the reference phase accumulator, the phase detector
5 containing circuitry to compute a difference between the reference phase and a variable phase;
6 a digitally-controlled oscillator (DCO) coupled to the phase detector, wherein the
7 performance of the DCO can be ascertained by observing an output of the phase detector; and
8 a variable phase accumulator coupled to the DCO and the phase detector, the variable
9 phase accumulator containing circuitry to compute the variable phase.

1 42. The circuit of claim 41 further comprising a time-to-digital converter (TDC) coupled to
2 the DCO and the phase detector, the TDC containing circuitry to compute a time difference
3 between a reference clock and a variable clock.

1 43. The circuit of claim 41 further comprising a loop filter coupled to the phase detector and
2 the DCO, the loop filter to provide a desired amount of attenuation to the computed difference
3 between the reference phase and the variable phase.

1 44. The circuit of claim 43, wherein the loop filter is of a type selected from a group
2 consisting of a finite impulse response filter, an infinite impulse response filter or combination
3 thereof.

1 45. The circuit of claim 44, wherein the loop filter is comprised of a plurality of filters, and
2 wherein the filters are arranged in a parallel fashion.

1 46. The circuit of claim 44, wherein the loop filter is comprised of a plurality of filters, and
2 wherein the filters are arranged in a cascaded fashion.

1 47. The circuit of claim 41 further comprising a gain normalization unit coupled to the phase
2 detector and the DCO, the gain normalization unit to normalize the difference between the
3 reference phase and the variable phase with respect to a gain in the DCO.